



PBDTA114ET

50 V, 100 mA low V_{CEsat} PNP resistor-equipped transistor;
 $R1 = 10\text{ k}\Omega$, $R2 = 10\text{ k}\Omega$

9 October 2025

Product data sheet

1. General description

PNP low V_{CEsat} energy efficient Resistor-Equipped Transistor (RET) in a small SOT23 Surface-Mounted Device (SMD) plastic package.

NPN complement: PBDTC114ET

2. Features and benefits

- Low collector-emitter saturation voltage V_{CEsat}
- High collector current gain (h_{FE})
- High energy efficiency due to less heat generation
- Improved device reliability due to reduced heat generation
- Built-in bias resistors
- Reduces component count
- Reduces pick and place costs
- Simplifies circuit design

3. Applications

- Digital applications in industrial segments
- Battery-driven low power devices
- Load-switches
- Low current drivers
- Power management and charging circuits

4. Quick reference data

Table 1. Quick reference data

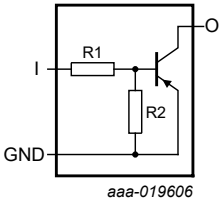
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CEO}	collector-emitter voltage	open base		-	-	-50	V
I_O	output current			-	-	-100	mA
R1	bias resistor 1 (input)	$T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	7	10	13	k Ω
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	

[1] See "Section 11: Test information" for resistor calculation and test conditions.

50 V, 100 mA low VCEsat PNP resistor-equipped transistor; R1 = 10 kΩ, R2 = 10 kΩ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	 SOT23	 aaa-019606
2	GND	ground (emitter)		
3	O	output (collector)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBDTA114ET	SOT23	plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PBDTA114ET	%5Y

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CBO}	collector-base voltage	open emitter		-	-50	V
V _{CEO}	collector-emitter voltage	open base		-	-50	V
V _{EBO}	emitter-base voltage	open collector		-	-10	V
V _I	input voltage			-40	10	V
I _O	output current			-	-100	mA
I _{OM}	peak output current	single pulse; t _p ≤ 1 ms		-	-200	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	250	mW
			[2]	-	350	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 μm copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.

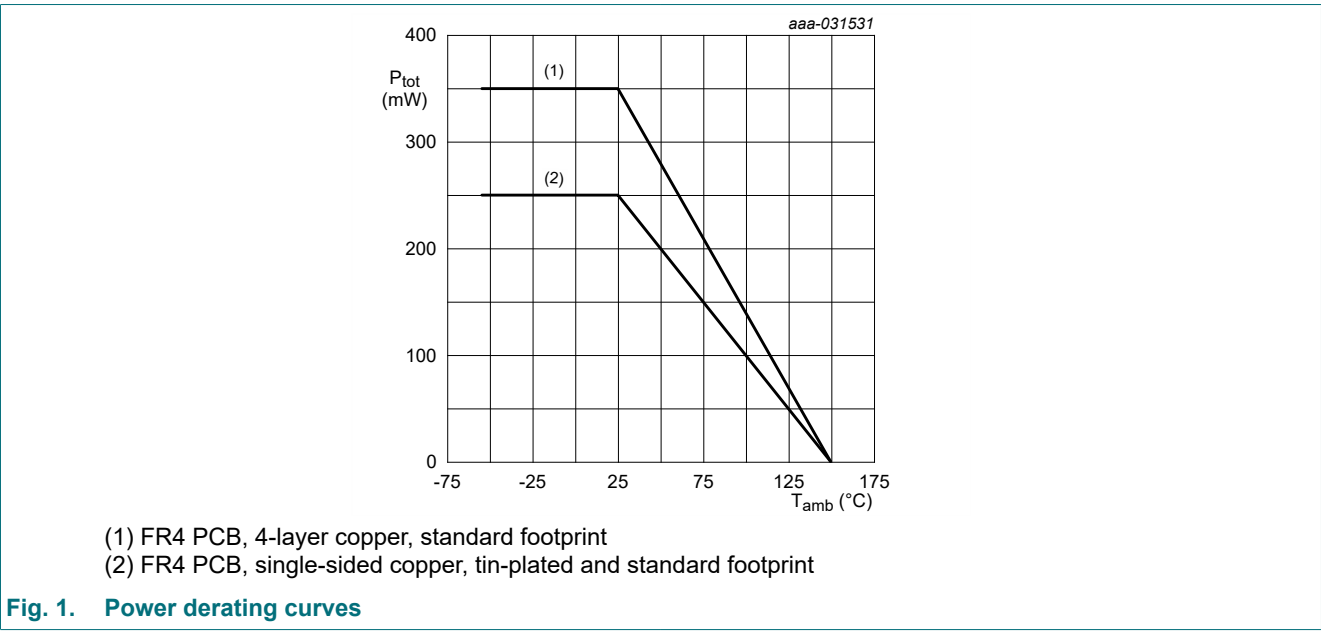


Fig. 1. Power derating curves

9. Thermal characteristics

Table 6. Thermal characteristics

Tamb = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Rth(j-a)	thermal resistance from junction to ambient	in free air	[1]	-	-	500	K/W
			[2]	-	-	357	K/W
Rth(j-sp)	thermal resistance from junction to solder point			-	-	130	K/W

- [1] Device mounted on an FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.

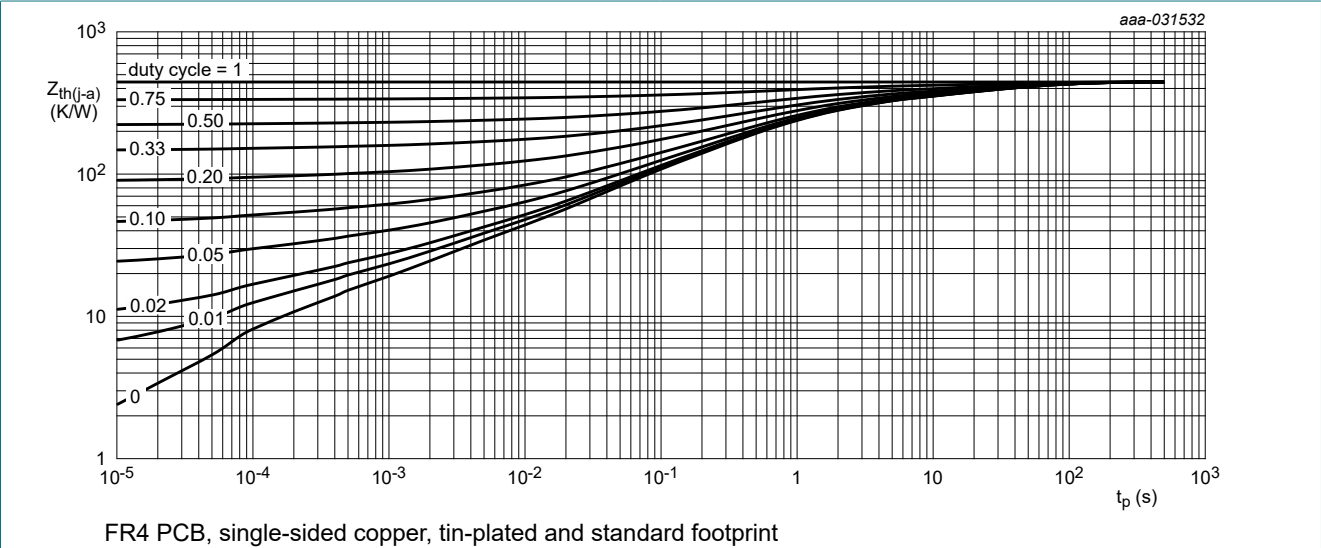


Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

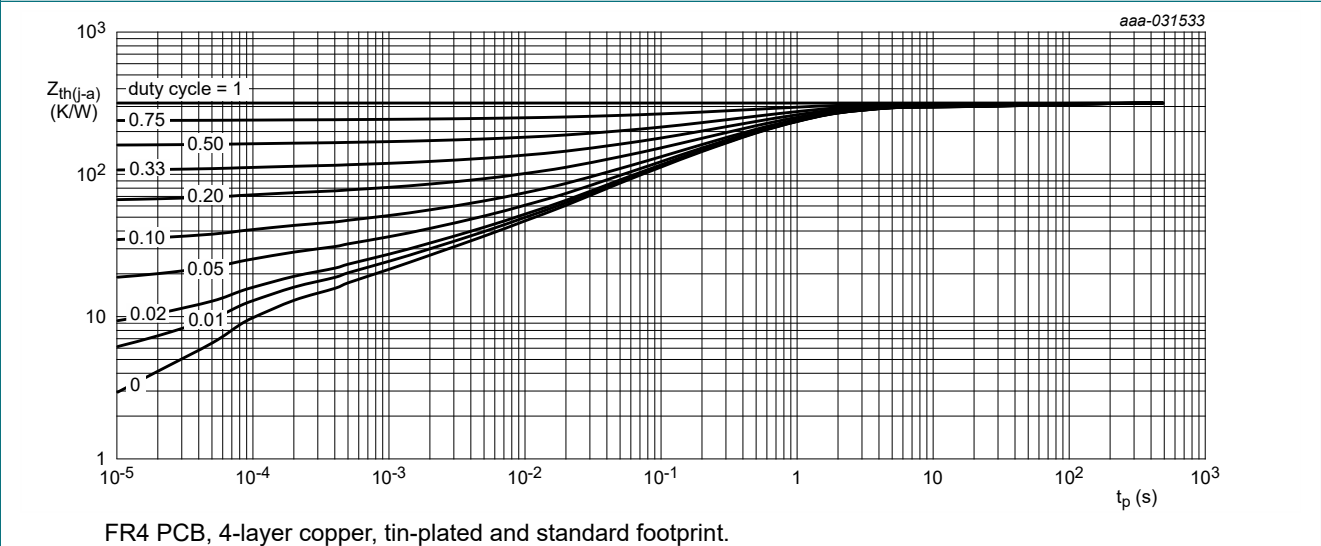


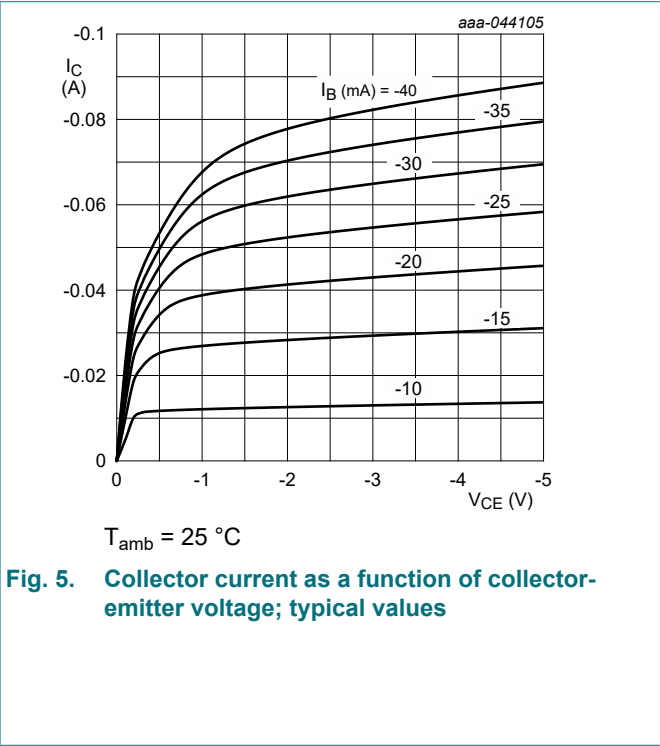
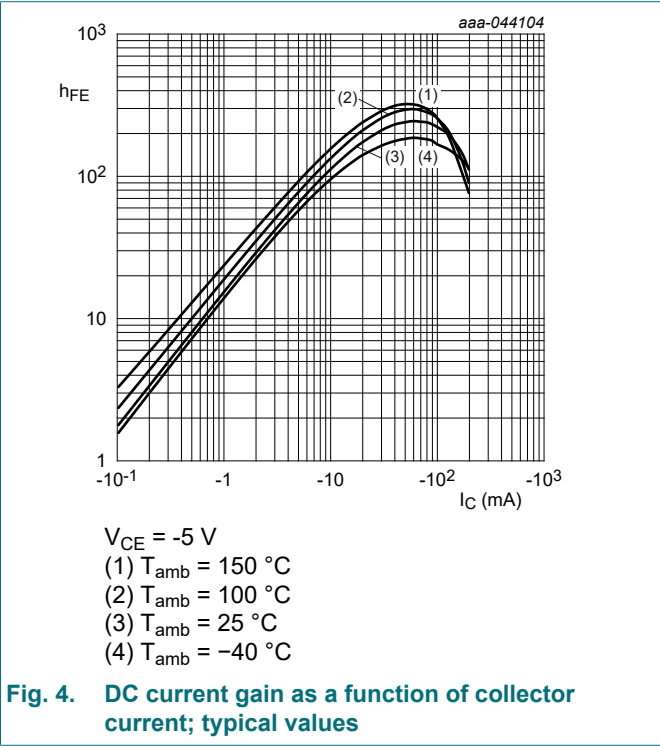
Fig. 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = -100\text{ }\mu\text{A}$; $I_E = 0\text{ A}$; $T_{amb} = 25\text{ }^\circ\text{C}$	-50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = -2\text{ mA}$; $I_B = 0\text{ A}$; $T_{amb} = 25\text{ }^\circ\text{C}$	-50	-	-	V
I_{CBO}	collector-base cut-off current	$V_{CB} = -50\text{ V}$; $I_E = 0\text{ A}$; $T_{amb} = 25\text{ }^\circ\text{C}$	-	-	-100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = -30\text{ V}$; $I_B = 0\text{ A}$; $T_{amb} = 25\text{ }^\circ\text{C}$	-	-	-100	nA
		$V_{CE} = -30\text{ V}$; $I_B = 0\text{ A}$; $T_j = 150\text{ }^\circ\text{C}$	-	-	-5	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5\text{ V}$; $I_C = 0\text{ A}$; $T_{amb} = 25\text{ }^\circ\text{C}$	-	-	-400	μA
h_{FE}	DC current gain	$V_{CE} = -5\text{ V}$; $I_C = -10\text{ mA}$; $T_{amb} = 25\text{ }^\circ\text{C}$	75	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -10\text{ mA}$; $I_B = -0.5\text{ mA}$; $T_{amb} = 25\text{ }^\circ\text{C}$	-	-	-100	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = -5\text{ V}$; $I_C = -100\text{ }\mu\text{A}$; $T_{amb} = 25\text{ }^\circ\text{C}$	-	-1.1	-0.8	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = -0.3\text{ V}$; $I_C = -10\text{ mA}$; $T_{amb} = 25\text{ }^\circ\text{C}$	-2.5	-1.8	-	V
R1	bias resistor 1 (input)	$T_{amb} = 25\text{ }^\circ\text{C}$	[1]	7	10	kΩ
R2/R1	bias resistor ratio		[1]	0.8	1	
C_c	collector capacitance	$V_{CB} = -10\text{ V}$; $I_E = 0\text{ A}$; $i_e = 0\text{ A}$; $f = 1\text{ MHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$	-	-	3	pF
f_T	transition frequency	$V_{CE} = -5\text{ V}$; $I_C = -10\text{ mA}$; $f = 100\text{ MHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$	[2]	200	-	MHz

[1] See "Section 11: Test information" for resistor calculation and test conditions.
[2] Characteristics of built-in transistor.



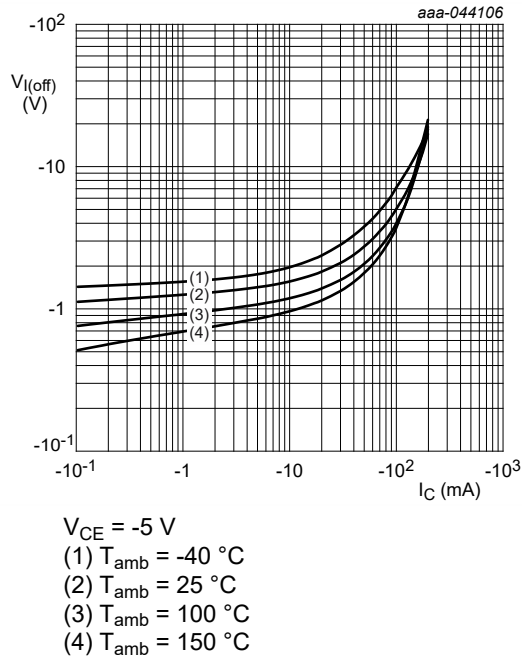


Fig. 6. Off-state input voltage as a function of collector current; typical values

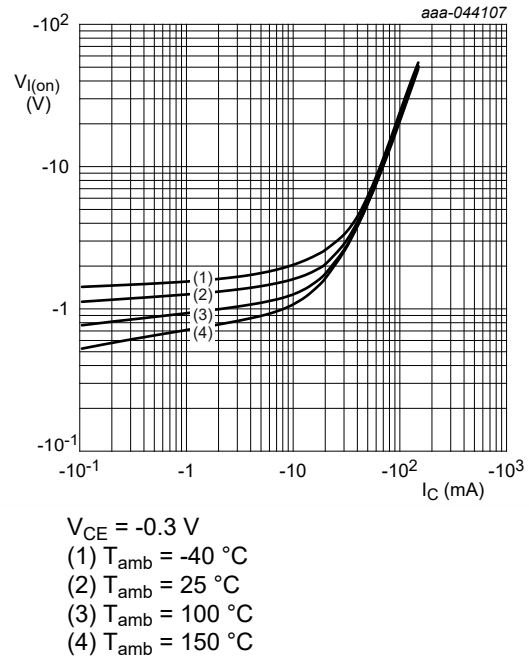


Fig. 7. On-state input voltage as a function of collector current; typical values

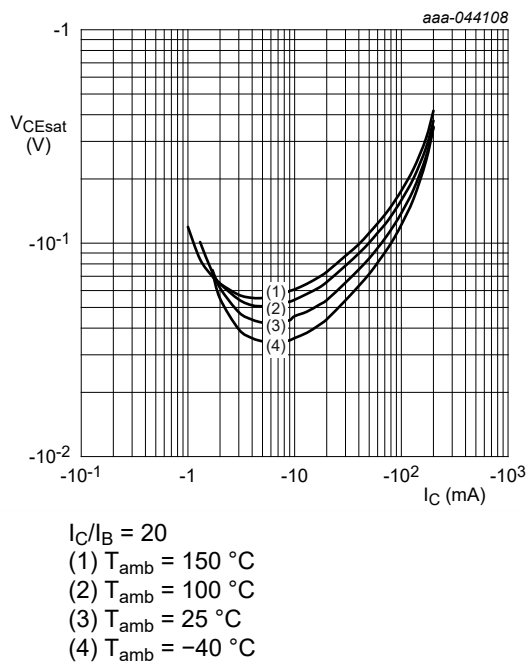


Fig. 8. Collector-emitter saturation voltage as a function of collector current; typical values

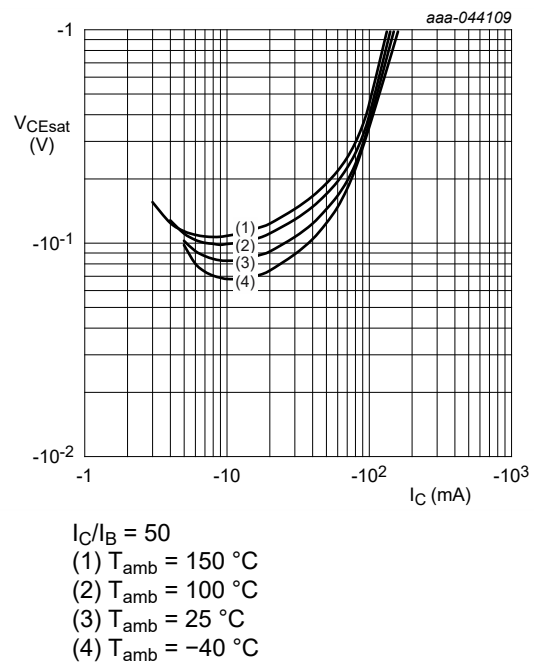


Fig. 9. Collector-emitter saturation voltage as a function of collector current; typical values

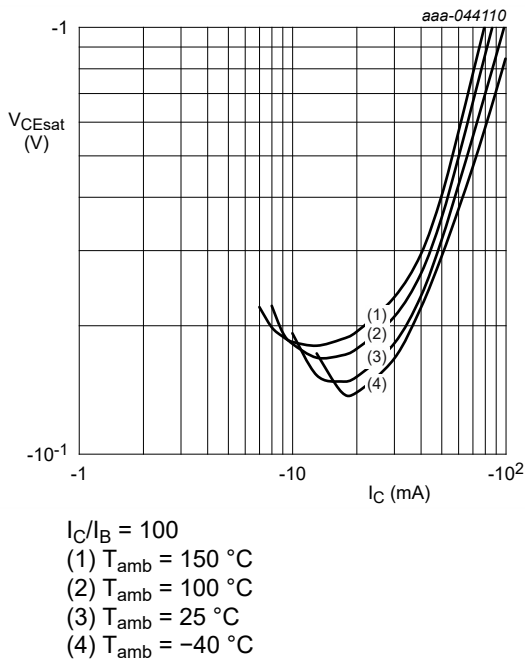


Fig. 10. Collector-emitter saturation voltage as a function of collector current; typical values

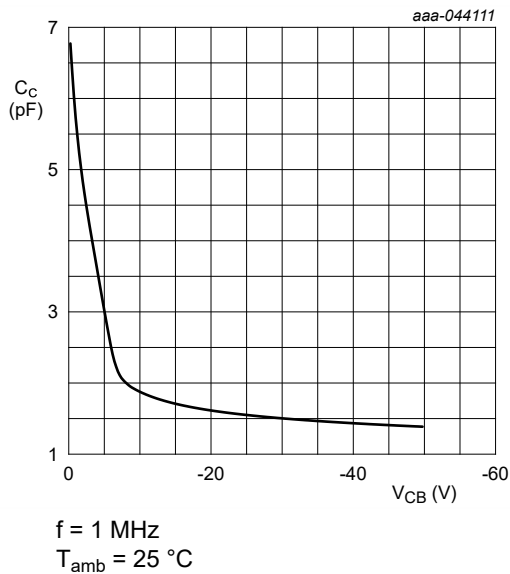
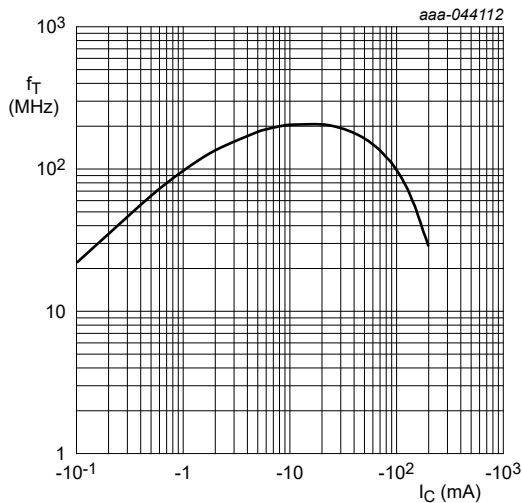


Fig. 11. Collector capacitance as a function of collector-base voltage; typical values



$f = 100\text{ MHz}$
 $T_{amb} = 25\text{ }^{\circ}\text{C}$
 $V_{CE} = -5\text{ V}$

Fig. 12. Transition frequency as a function of collector current; typical values of built-in transistor

11. Test information

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R_2}{R_1} = \frac{V(I_4) - V(I_3)}{R_1 \cdot (I_4 - I_3)} - 1$$

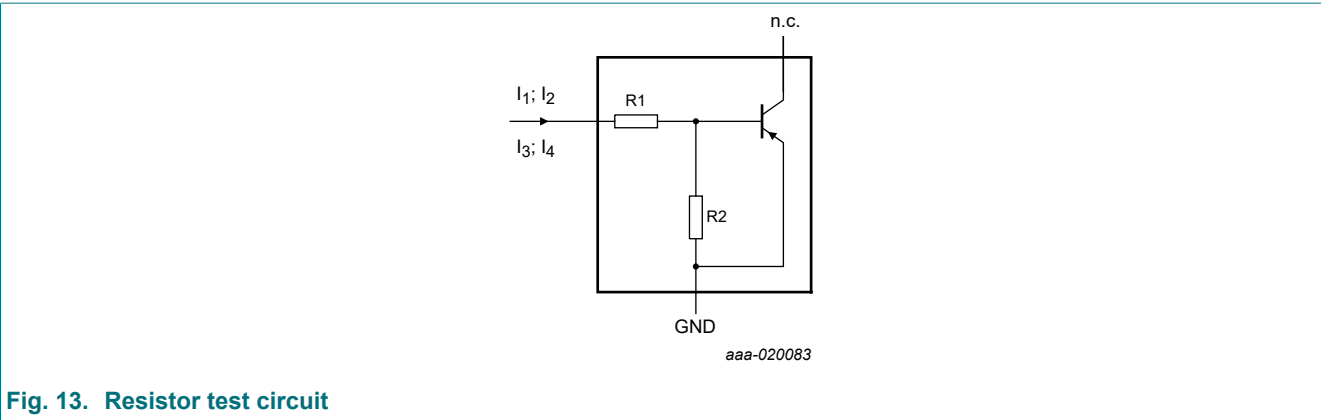


Fig. 13. Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I1	I2	I3	I4
PBDTA114ET	10	10	-800 μA	-1100 μA	350 μA	450 μA

12. Package outline

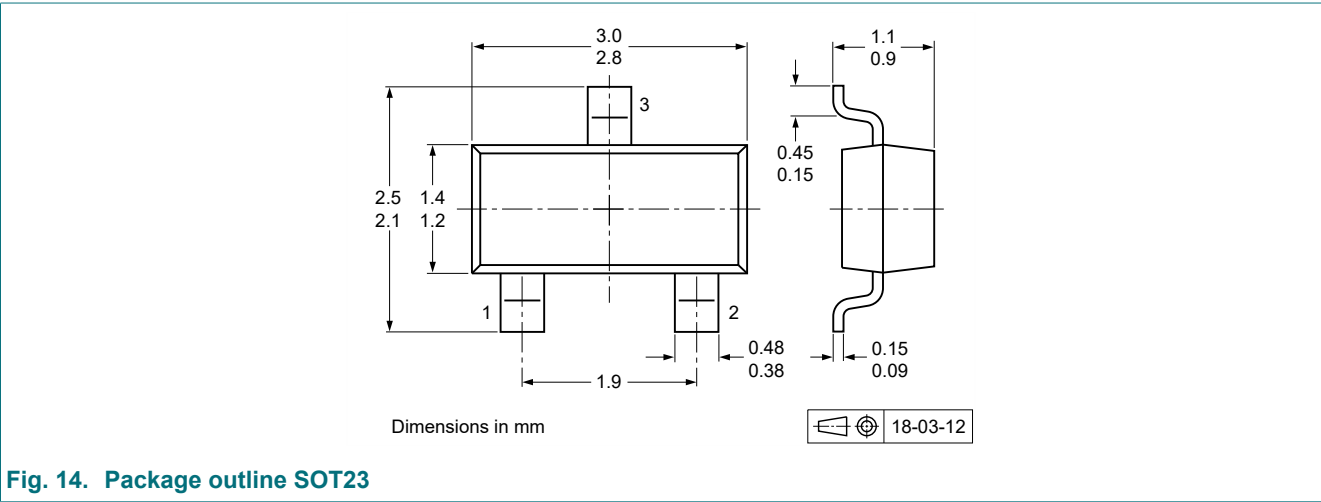


Fig. 14. Package outline SOT23

13. Soldering



Fig. 15. Reflow soldering footprint for SOT23

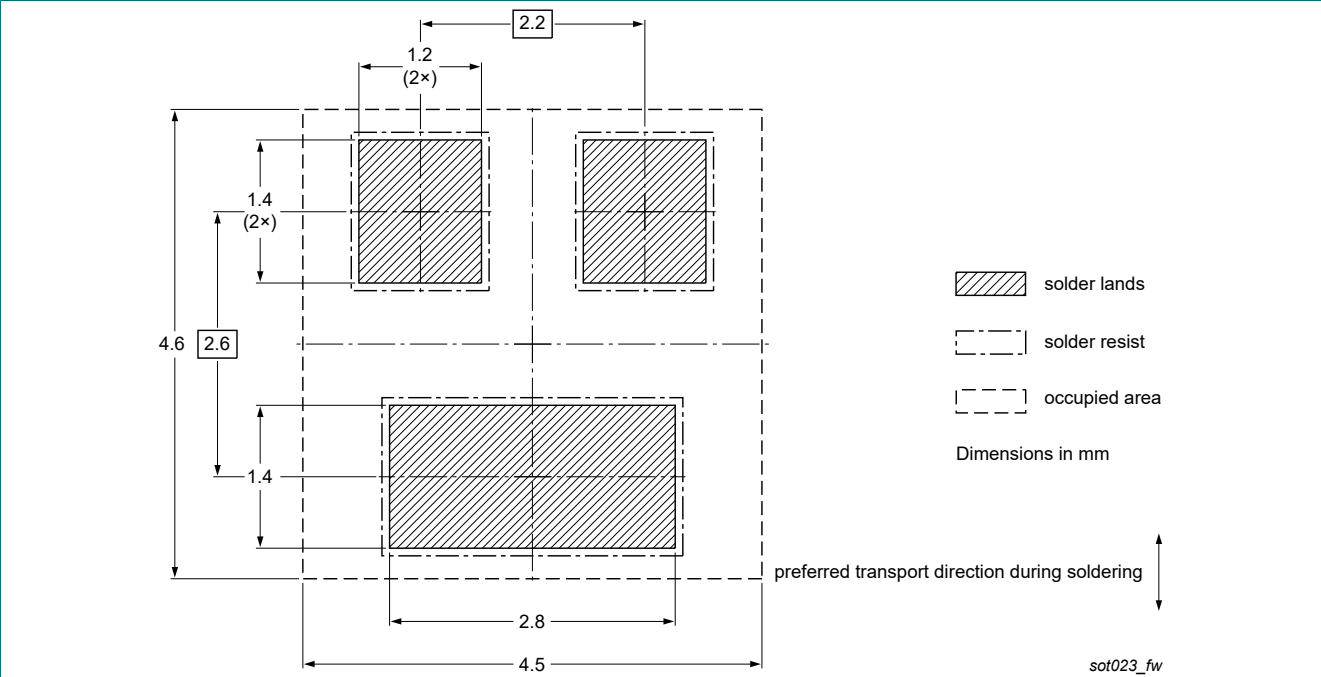


Fig. 16. Wave soldering footprint for SOT23

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBDA114ET v.1	20251009	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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